TF-480
Wire Speed NAT Router SOC
Datasheet

DS_TF-480_001R001
Version: 0.9
2007/11/25

Revision History

Revision	Date	Change Description
DS_TF-480_001R001	11/25/2007	Preliminary

Contents

1. Description

Taifatech's **TF-480** Silicon NAT Accelerator delivers the highest performance possible in network address translations for SOHO routers, Home Gateways or even some telecom routers. 100Mbps full duplex LAN-WAN wire-speed performance is achieved by embedding the NAT and many other functions into hardware. The **TF-480** has two built-in 10/100 MAC and a pipelined RISC CPU. The **TF-480** also offers features usually found in high-end systems such as QoS, Rate Control, IP multicast forwarding table, multi-session PPPoE with fault tolerance.

With the emergence of the entertainment network and also the development of the Digital Home concept, large number of Internet enabled nodes are being added to the network. By bringing Network Address Translation performance to a new plateau, the **TF-480** increases the overall system performance in communication and Internet appliances, and Smart Objects aimed for the broadband environment.

The hardware based multicast pass through from WAN to LAN function delivers an ideal solution for ISP who place IP STB into users home and the free video is streamed by multicast packets. The TF-480 supports up to 32 IGMP groups with 32 IP address each.

The **TF-480** allows advanced features such as QoS, Rate Control, IP multicast forwarding, multi-session PPPoE, multi-WAN and load balancing found only in high-end routers to be implemented into the design, therefore enabling a new breed of high performance, high availability and feature rich routers for the SOHO market or some telecom application at an affordable price.

2. Features

2. 1. Network Address Translation

- **NAT features**
  - Hardware based NAT/NAPT, 4K entries for NAT table
  - Supports up to 8 public IP addresses
  - Supports up to 8 DMZ hosts

- Supports port range forwarding, up to 24 entries
- Support port forwarding, up to 32 entries
- Supports port range triggering, up to 24 entries
- Supports PPTP, L2TP and IPsec Pass through
- Supports VLAN tag packet pass through from WAN to LAN
- Supports either symmetric type or cone type NAT
- Supports optional maximum NAT session limitation to 512 sessions per IP

- **Hardware based Layer 2 bridging, 512 entries for L2 routing table**
- **Hardware based Layer 3 routing, 256 entries for LAN and 128 entries for WAN IP table**
- **Supports up to 4 LAN Static Route entries**
- **Supports up to 4 WAN Static Route entries**
- **Supports up to 32 groups and 32 IP for each group IP Multicast Pass Through from WAN to LAN**
- **Hardware based packet filtering**
    - Port filtering, up to 10 port numbers
    - IP filtering, up to 256 source IP addresses and 30 destination IP addresses
    - Source and Destination MAC address filtering, up to 512 MAC addresses
- **Egress or Ingress rate control on WAN port**
- **4 session hardware based full wire speed PPPoE**

2. 2. MCU and Peripherals

- **MCU**
    - Pipelined RISC TF-390 core, 50MHz operating frequency, single cycle per instruction
    - Software compatible with standard 8051
    - Embedded 16K SRAM for data memory or program mirror
    - Supports 32KB/64KB program mirror in internal SRAM which can be mapped to any programming memory range
    - Supports up to total 4MB External Flash/ROM/SRAM
    - Supports 4 channel DMA
    - Support 8/16 bit mode IO DMA
    - Provides two 128 byte Linear Access Windows
    - Three 8-bit GPIOs

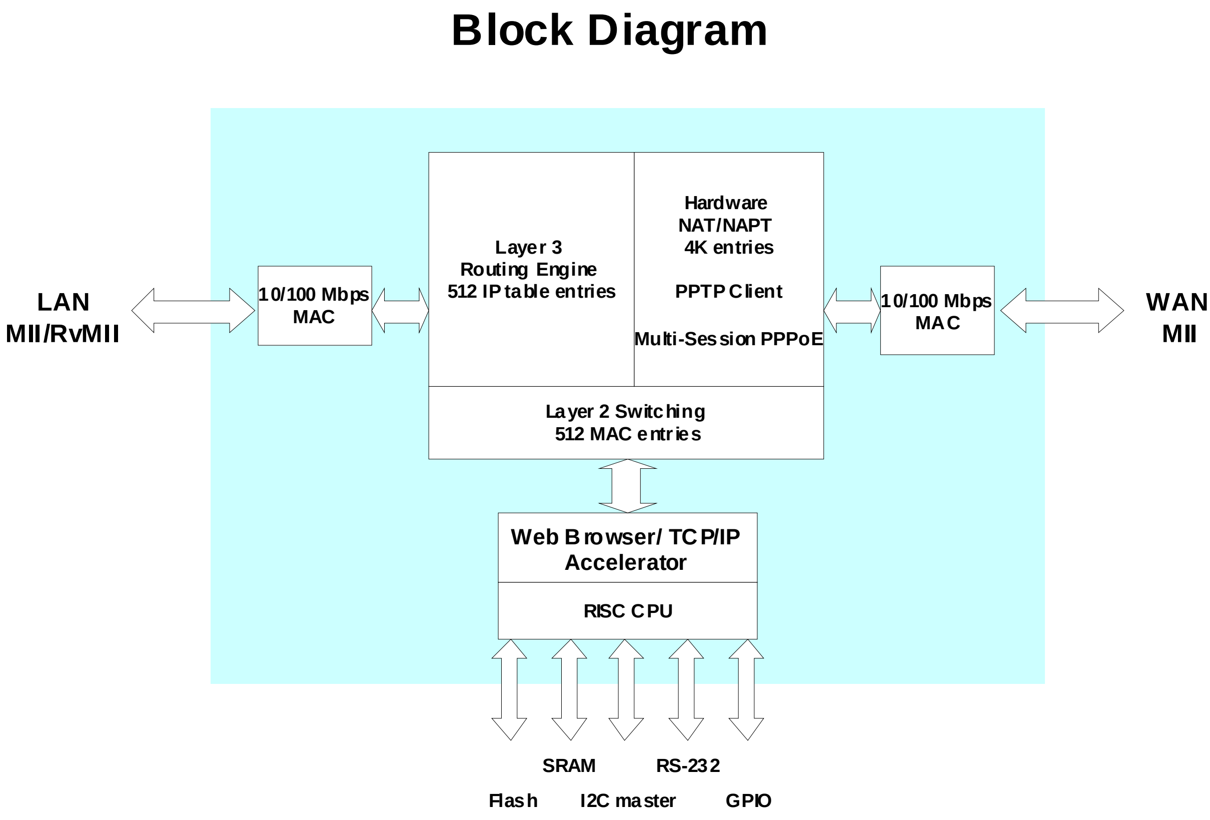
- Software Code protect
- I2C slave interface

- **Dedicated 22-bit address and 8-bit data bus for external program, data memory and extended IO**
- **Built-in Internet Protocol Accelerator**
- **Hardware based 1 byte to 8 byte pattern search engine**
- **Per port real time pattern search.**
- **Online Firmware Upgrade through TFTP or HTTP (web browser)**

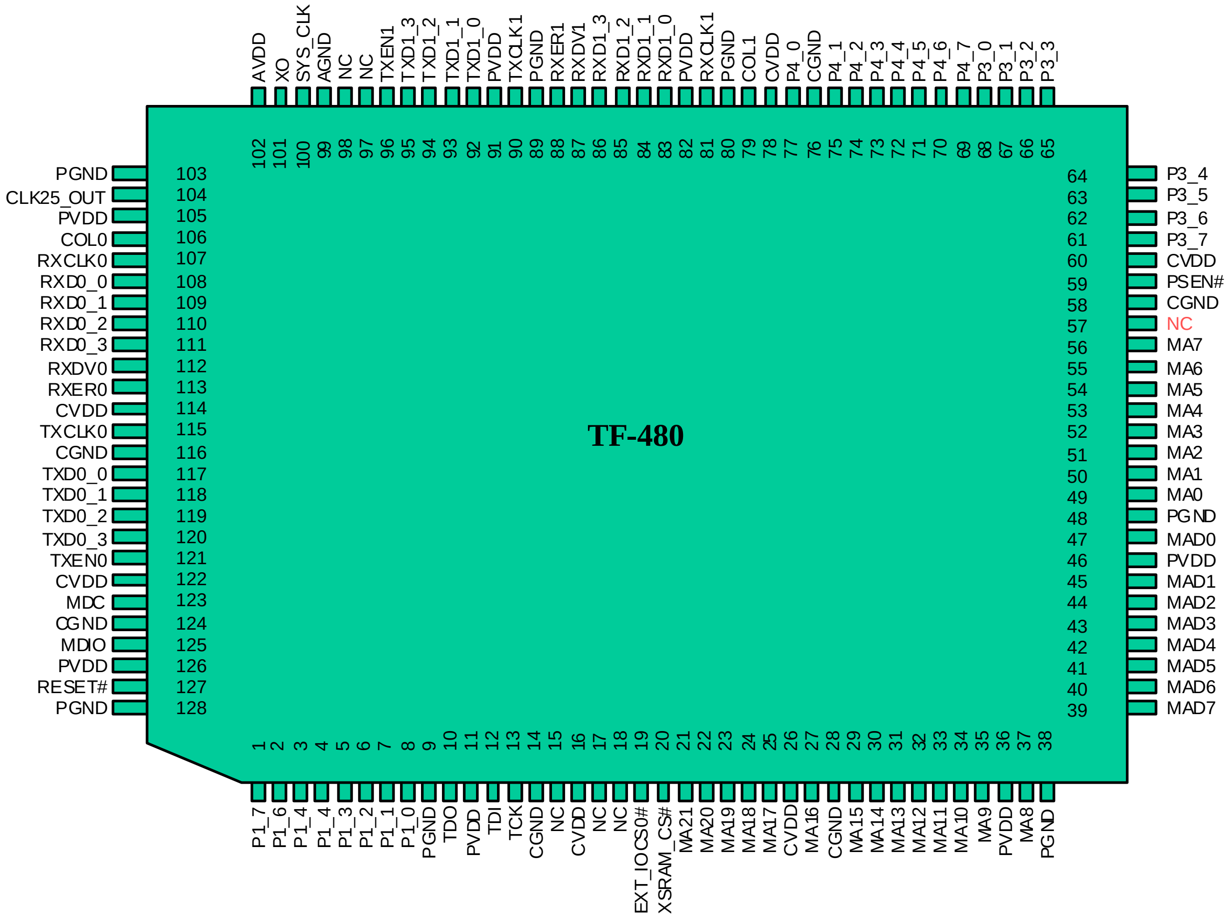
2. 3. MISC

- **Embedded 2 Ethernet MAC for LAN and WAN each**
  - Selectable MII or Reverse MII interface on LAN, MII on WAN
  - 802.3x flow control for full duplex mode and Jamming for half duplex mode
- **Embedded 194K bytes SRAM for packet buffer, MCU data memory, L2/L3 address table and NAT table.**
- **One 25MHz clock output for external PHY**
- **50MHz system clock crystal or oscillator input**
- **0.18 um CMOS technology, 1.8V internal operation, 3.3V IOs**
- **128-pin QFP package**

3. Block Diagram



4. Pin Description



4. 1. Memory/Peripheral Interface

Pin Name	No.	Type	Description
N_PSEN	59	O	**Program Store Enable Output**. This signal is commonly connected to optional external program memory as a chip enable. N_PSEN provides an active low pulse and gives high when external program memory is not being accessed.
MA [21:16]	21,22,23 24,25, 27	IU/O	Address bus. Should pull up these pins externally.
MA[15:8]	29,30,31, 32,33,34, 35,37	O	Address bus
MA[7:0]	56,55,54, 53,52,51, 50,49	IU/O	Address bus Should pull up these pin externally.
MAD [7:0]	39,40,41, 42,43,44, 45,47	I/O	Data bus
N_XSRAM_CS	20	O	**External SRAM chip select**
N_IOCS0	19	O	**Extended IO 0 Chip Select,** active low

4. 2. Port #0 (WAN port) MII Interface (14 pins)

Pin Name	No.	Type	Description
TXD0 [3:0]	120,119, 118,117	O	**Transmit Data.** The TF-480 will source TXD0 [3:0] synchronous with TXCLK0 when TXEN0 is asserted.
TXCLK0	115	I	**Transmit Clock.** Continuous (25MHz/2.5MHz) clock input which is used to synchronize TXEN1 and TXD1 [3:0].
TXEN0	121	O	**Transmit Enable.** Indicates the MAC has presented valid data on the TXD1 [3:0].
RXD0 [3:0]	111,110, 109,108	I	**MII Receive Data.** The external PHY will source RXD1 [3:0] synchronous with RXCLK0 when RXDV1 is asserted.
RXCLK0	107	I	**MII Receive Clock.** Continuous (25MHz/2.5MHz) clock input which is used by the MAC to synchronize RXDV1, RXD1 [3:0] and RXER1.
RXDV0	112	I	**MII Receive Data Valid.** While RXDV0 is asserted, it means the external PHY has presented valid recovered data on the RXD0 [3:0].
RXER0	113	ID	**Receive Error.** Indicates the external PHY has received invalid symbol data.
COL0	106	I	**MII Collision Detection.** Active when collision is detected.

4. 3. Port #1 (LAN port) MII Interface (14 pins)

Pin Name	No.	Type	Description
TXD1[3:0]/ RvRXD[3:0]	95, 94, 93, 92	O	**Transmit Data.** The TF-430 will source TXD1 [3:0] synchronous with TXCLK1 when TXEN1 is asserted. **Reverse Receive Data**. The TF-430 will source RvRXD [3:0] synchronous with RvRXCLK when RVRXDV is asserted.
TXCLK1/ RvRXCLK	90	I/O	**MII Transmit Clock.** Continuous (25MHz/2.5MHz) clock input used to synchronize TXEN1 and TXD1 [3:0]. **Reverse MII Receive Clock**. Continuous (25MHz/2.3MHz) clock output used to synchronize RvRXDV and RvRXD [3:0].
TXEN1/ RvRXDV	96	O	**Transmit Enable.** Indicates the MAC has presented valid data on the TXD1 [3:0]. **Reverse Receive Data Valid**. Indicates TF-480 has presented valid data on the RvRXD [3:0].
RXD1[3:0]/ RvRXD[3:0]	86, 85, 84, 83	I	**MII Receive Data.** The external PHY will source RXD1 [3:0] synchronous with RXCLK1 when RXDV1 is asserted. **Reverse MII Transmit Data**. The external Device (MAC) will source RvTXD [3:0] synchronous with RvTXCLK when RvTXEN is asserted.
RXCLK1/ RvTXCLK	81	I/O	**MII Receive Clock.** Continuous (25MHz/2.5MHz) clock input which is used by the MAC to synchronize RXDV1, RXD1 [3:0] and RXER1. **Reverse MII Transmit Clock** (output)
RXDV1/ RvTXEN	87	I	**MII Receive Data Valid.** The external PHY has presented valid recovered data on the RXD1 [3:0] **Reverse MII Transmit Enable** (input)
RXER1	88	ID/O	**Receive Error.** Indicates the external PHY has received invalid symbol data.
COL1	79	I/O	**MII Collision Detection.** Active when collision is detected. **Reverse Collision Detection** (output)

4. 4. MDC/MDIO Interface (2 pins)

Pin Name	No.	Type	Description
MDC	123	O	**Management Transmit Clock**
MDIO	125	I/O	**Management Transmit Data IO**

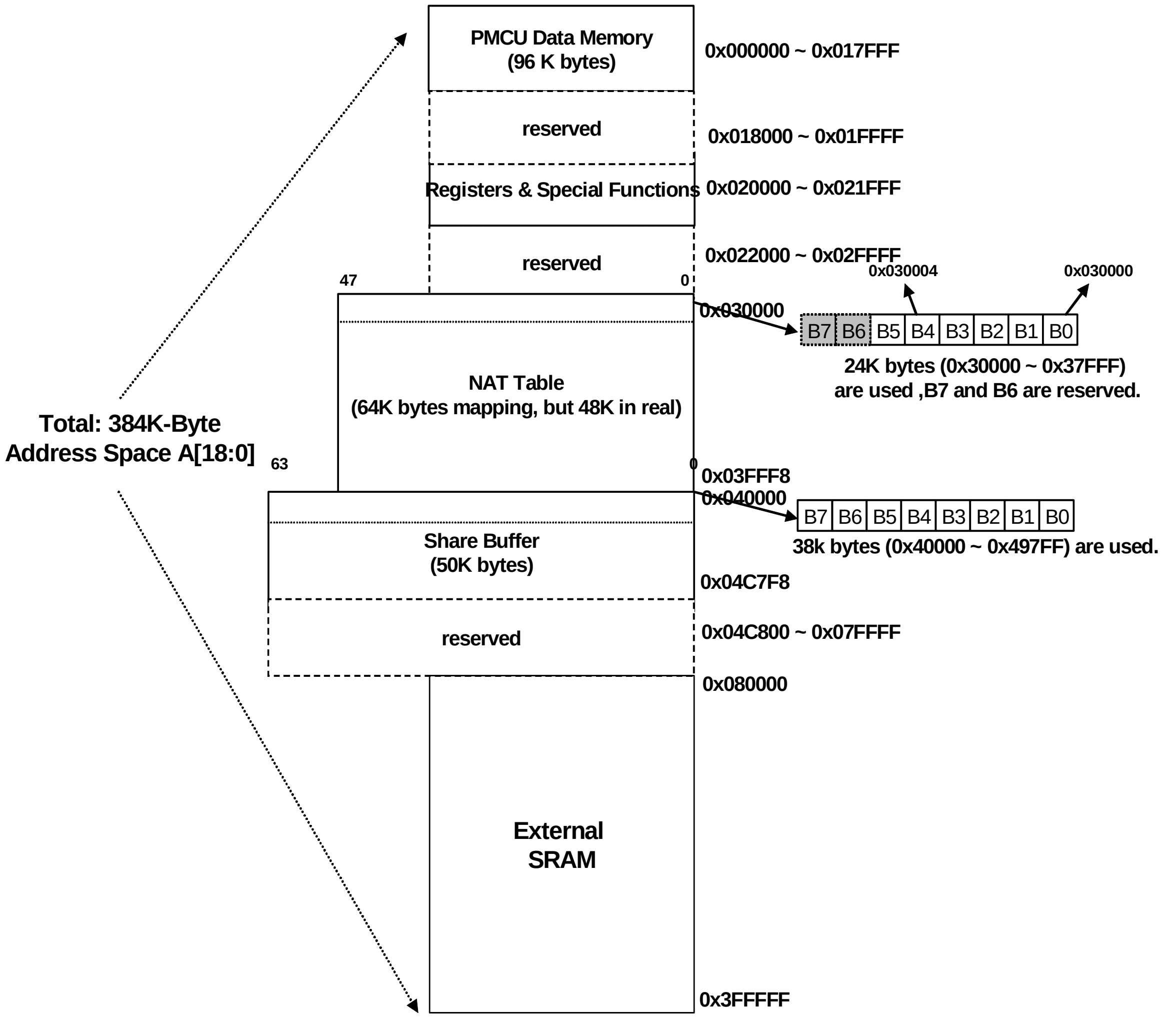
4. 5. Global IOs (24 pins)

Pin Name	No.	Type	Description
P1.7 –N_IODMA_RDY P1.6 P1.5 P1.4 –N_XFL_WR P1.3 P1.2 P1.1 P1.0	1,2,3,4 ,5,6,7, 8	IU/O	Port 1. 8-bit bi-directional I/O port. Alternate functions: N_IODMA_RDY: IO DMA Ready input N_XFX_WR: External Flash Write strobe output, active low
P3.7 – N_XSRAM_RD P3.6 – N_XSRAM_WR P3.5 – T1 P3.4 – T0 P3.3 – N_INT1 P3.2 – P3.1 – STXD P3.0 – SRXD	61,62, 63,64, 65,66, 67,68	IU/O	T1 should be open collector Alternate functions: N_XSRAM_RD: External Data Memory read strobe output, active low N_XSRAM_WR: External Data Memory Write strobe output, active low T1: Timer 1 external input T0: Timer 0 external input N_INT1: External Interrupt input 1, active low STXD: Serial Port Transmit output SRXD: Serial Port Receive input
P4.7 P4.6 P4.5 P4.4 P4.3 P4.2 P4.1 P4.0	69,70, 71,72, 73,74, 75,77	IU/O	Port 4. 8-bit bi-directional I/O port.

4. 6. Miscellaneous (9 pins)

Pin Name	No.	Type	Description
N_RST	127	I	System Reset. Active low
CLK – XI	100	I	Clock Input or Crystal Input
XO	101	O	Crystal Output
TCK	13	O	Test Clock output
TDI	12	I	Test Data Input
TDO	10	O	Test Data Output,
CLK25_OUT	104	O	25MHz clock output
reserved	97, 98		Reserved, should tie to ground.
NC	15, 17, 18, 57		No Connection
AVDD	102		3.3V Analog VDD
AGND	99		Analog Ground
PVDD	11,36,46,82, 91,105,126		3.3V IO VDD
PGND	9,38,48,80,89 ,103,128		IO GND
CVDD	16,26,60,78, 114,122		1.8V Core VDD
CGND	14,28,58,76, 116,124		Core GND

5. Address Mapping



The data memory address mapping is indicated in the above figure.
0x000000 to 0x017FFF is the 96K byte internal SRAM.
0x018000 to 0x01FFFF is reserved.
0x020000 to 0x021000 is for Linear Access Window.
0x021000 to 0x021FFF is for Registers.
0x00E000 to 0x02FFFF is reserved.
0x030000 to 0x03FFFF is the 4K entry NAT table.
0x040000 to 0x04C7FF is the 50KB shared buffer.
0x04C800 to 0x07FFFF is reserved.
0x080000 to 0x3FFFFF is mapped for external SRAM.

6. Functional Descriptions

The **TF-480** has 2 MACs with MII or RvMII interfaces. MAC#0 is for WAN port and MAC#1 is for LAN port. Layer 2 switching or layer 3 routing is performed packet forwarding between LAN and WAN interfaces. The **TF-480** also has a CPU interface which is connected to its embedded 8-bit pipeline RISC CPU, and some hardware functions, such as 5-channel DMA, hardware checksum generator and inspector, hardware NAT and hardware PPPoE etc. to accelerate network protocols processing.

In this chapter, we will give a more detail description on each functions provided by **TF-480.**

6. 1. Initialization

Initially, the link between the two MII interfaces (WAN and LAN) are turned off, and their TX and RX are disabled. To enable data passing through these two interfaces, we should turn on their corresponding **Link_on** bits, **RX_enable** bits and **TX_enable** bits in **MAC Control and Configure** registers (for details please refer TF480 programming guide**)**.

6. 2. Pure 2 Port Switch Mode

The **TF-480** can operate as a pure 2-port switch. In this mode all packets are forwarded based on its MAC address. To enable this mode, you have to turn off L3 routing function and turn on bridge mode in of **Routing Control** register. For details please refer **TF480 programming guide**.

6. 3. NAT Router mode

The **TF-480** operates mainly as a NAT Router. In this mode all packets are forwarded based on their layer 3 and/or even layer 4 information. The **TF-480** can also operate as a basic Router. In this mode, NAT is disabled and all packets are processed by CPU of **TF-480**.

6. 4. NAT Function

As a NAT router, the **TF-480** always performs NAT function. The NAT function not only translates the IP address from private IP to public IP but also map the port number of TCP or UDP packet or ID of ICMP packet to a pseudo number. To enable NAT, turn on L3 bit of **Switch Control 0** register and configure the **Pseudo_port_offset** so that the pseudo port number will fall into a suitable range.

6. 5. Port Range Triggering

The **TF-480** provides Port or Port Range Triggering function. Up to 24 ranges can be defined for triggering by configuring registers from **0x21200~0x212BC**. Each port or port range is defined by 5 registers: 2 registers to define the upper bound of the range, 2 registers to define the lower bound of the range and one register to define protocol and direction of port triggering. For details please refer **TF480 programming guide**.

6. 6. DMZ Function

The **TF-480** provides up to 8 DMZ hosts. Each DMZ host maps to one **MY_WAN_IP.** This means if one DMZ host is used, only **MY_WAN_IP0 is needed** for WAN interface; and if 2 DMZ hosts are used, **MY_WAN_IP0** and **MY_WAN_IP1** need to be configured for WAN interface and so on and so forth.

6. 7. VPN Pass Through

The **TF-480** supports VPN pass through function which allows VPN packets, such as ESP, PPTP and L2TP packets, to pass through this NAT device. Some registers related to the VPN pass through function are **ESP_IP Register**, **ESP_AGING Register**, **PPTP_IP Register**, **PPTP_AGING Register**, **L2TP_IP Register** and **L2TP_AGING Register**. For details please refer **TF480 programming guide**.

6. 8. Source MAC, Destination MAC, Source IP, Destination IP and Destination Port Filtering Function

The **TF-480** provides several filtering scheme, namely Source MAC filtering, Destination MAC filtering, Source IP filtering, Destination IP filtering and Destination Port filtering. All these filtering functions work independently. Once any one of these filtering conditions is met, the packet is dropped or forwarded to the CPU according to the configuration of **Router Control Register**.

The **TF-480** uses the **layer 2 address table** to implement Source MAC and Destination MAC filtering function. Each entry of the layer 2 address table is 64 bit in width. There are total 512 entries for layer 2 address table and therefore, the **TF-480** provides up to 512 entries for Source MAC or Destination MAC filtering function.

The **TF-480** provides an asymmetric IP filtering feature only for packets from LAN. For Source IP filtering, the **TF-480** makes use of the **LAN IP table** to implement this function. The **TF-480** has 256 entries in LAN IP table, and therefore, it supports up to 256 Source IP Filtering. Notice that the Destination IP Filtering function is performed on the out bond WAN packets only, therefore, it will **NOT** be forwarded to CPU port even if the **Filt_fwd2cpu** is on.

The **TF-480** provides only 30 entries for Destination IP Filtering function, which is also asymmetric from LAN to WAN traffic only. Packets from LAN to WAN with destination IP address matches any one of the 30 entries will be filtered.

For Destination Port Filtering function, the **TF-480** provides 10-entry destination port filtering table, which allows asymmetric destination port filtering for TCP or UDP packets from LAN to WAN. Any TCP or UDP packets from LAN to WAN with destination IP which hit any entry in the table will be filtered.

6. 9. CPU Port RX & TX Packet

The CPU port can receive one packet at a time. The location of RX buffer can be defined by configuring the **RX Buffer Address registers.** When CPU is expecting a packet, it can either poll the **RX_BUF_OCP** bit **or RX_PKT** bit (for details please refer TF480 programming guide)**.** When either bit is set to one, it indicates one packet is received in the RX Buffer. **RX_packet_length registers** indicate the received packet length. Interrupt can also be used to inform the CPU of a RX packet. When a packet is received, an interrupt will be issued if the interrupt event triggering is enabled.

There are 2 sets of **TX Descriptor Registers**, **Descriptor 0** and **Descriptor 1.** Functions of these 2 sets of registers are the same. Hardware will transmit packets alternatively if either one set of descriptor is set.

6. 10. CPU Port RX Packet Filtering

There are several options for packets forwarded to the CPU either from LAN or from WAN. **CPU Port Packet Filtering Control #0** register and **CPU Port Packet Filtering Control #1** register control the on-off of these filtering functions.

6. 11. Virtual Server (Port Forwarding)

TF-480 provides 128 Virtual Server entries. The 32 of which are ranged port forwarding while 96 of which are for specific layer-4 port number. If the application needs a ranged layer-4 port number, we can use the first 24 entries in the virtual server table; and if the application uses a specific port number, we can use the rest 32 entries.

6. 12. QoS Function

The **TF-480** supports QoS based on the application. To use this function, we should first turn on the **QoS Enable bit** of the **Routing Control register.**

A **priority bit** in each Virtual Table entry can be turned on or off. Once the **priority bit** is turned on, traffic to that corresponding Virtual Server gets higher priority. The **TF-480** provides other 4 entry QoS table with QoS IP, QoS Port field and QoS valid registers. Traffic from LAN with source IP meets the QoS IP in this table or layer-4 destination port number equals to the QoS Port or both will be routed through priority path.

6. 13. PPPoE/Multi-Session PPPoE Function

The **TF-480** provides PPPoE and Multi-Session PPPoE function. Up to 4 PPPoE sessions are supported.

The TF-480 also provides a timer for PPPoE Session#0, for maintaining the PPPoE Session#0 connection in the case of connection on demand. Whenever a PPPoE packets passing through, this timer will be cleared to 0. Therefore, CPU can read the timer, increase and then write back to the timer register. If the timer reached a certain threshold value, that means the connection is currently no more needed, we can close the connection.

The TF-480 can support 3 more additional PPPoE sessions besides session#0. These 3 additional PPPoE sessions allow users to connect to other ISPs for some specific destination IPs (range) or source IPs (range) or both.

6. 14. Pattern Search

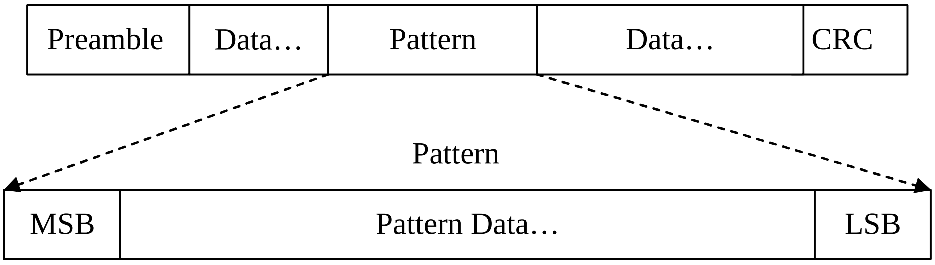
The **TF-480** provides a “Pattern Search” function to find a specific pattern in packets or data in the 16K data memory. You can define a pattern at most 64 bit wide, the search range, and then wait for the result. This function shares the DMA function interface and therefore it does not work concurrently with DMA function.

If the search is successful, the location of memory block will be stored in registers “Pattern location”, which shares the **CRC/Checksum Calculate Result** registers**.**

6. 15. Per Port Pattern Search

The **TF-480** provides a “Port Pattern Search” function for each WAN port and LAN port to find a specified pattern in packets. You can simply define a pattern (at most 32 bytes wide) and the desired search action. The hit packet can be dropped or forwarded to CPU. It supports three additional 16-byte patterns for LAN port to increase the search flexibility.

A packet hits the search pattern means that the packet contains a search pattern. A packet hits a pattern is showed below. The preamble and CRC data are ignored when pattern search is performed. The MSB (most significant byte) of the pattern is received earlier than the LSB (least significant byte). Please take care of the data order to define a correct pattern.



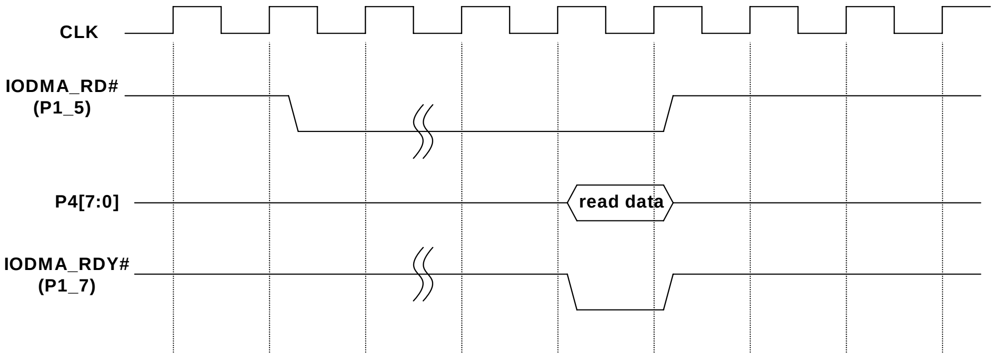
6. 16. DMA

The **TF-480** provides two mode DMA, one is “memory to memory DMA”, the other is “Flash to memory DMA”. The “memory” includes “on-chip memory”, “off-chip memory”, “off-chip IO device”. The “memory” address spaces are as follows:

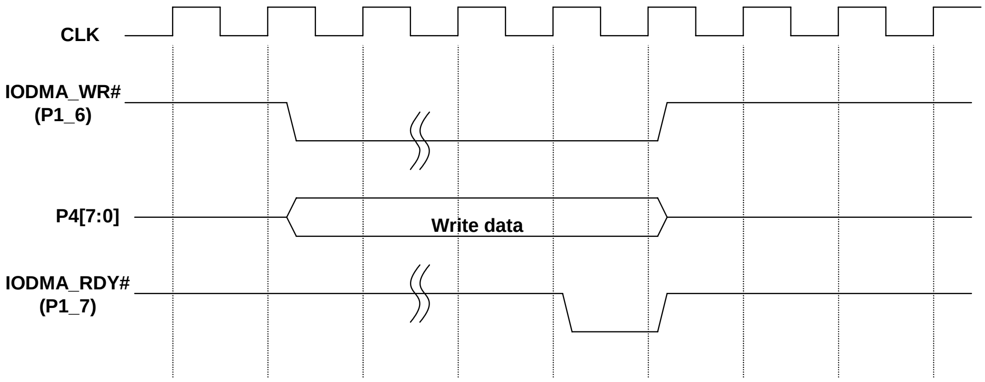
- On-chip memory (96KB): 0x000000 ~ 0x017FFF
- Off-chip memory (1.5MB): 0x080000 ~ 0x1FFFFF
- Off-chip IO device (2MB): 0x200000 ~ 0x3FFFFF

Software can use different “DMA source address” & “DMA destination address” to decide which “memory” will execute DMA function.

When data is moved from or to IO interface, GPIO port P4[7:0] is used as IO DMA data bus, P1[5] as active low IO DMA read control signal, P1[6] as active low IO DMA write control signal and P1[7] as active low IO DMA read/write ready indication. The timing diagram for IO DMA read write accesses is as follows:



IO DMA Read



IO DMA Write

Timing for external flash to internal memory DMA will follow the timing for accessing external flash read/write.

6. 17. MDC/MDIO

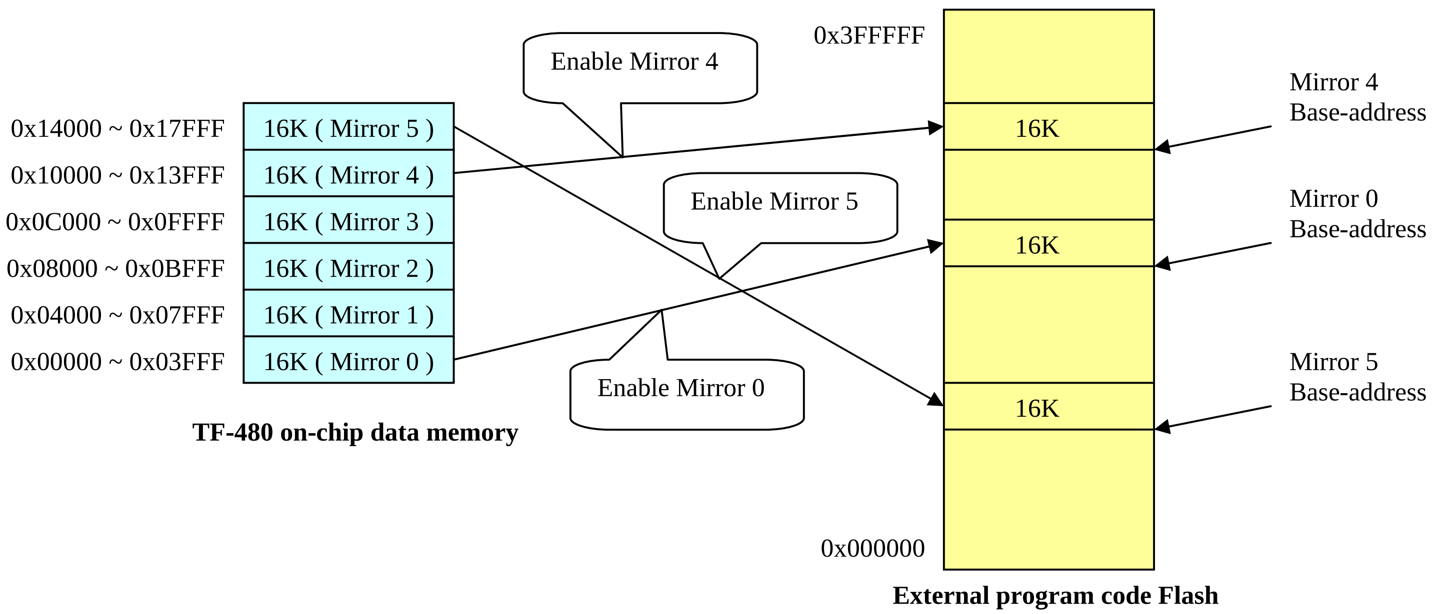
The **TF-480** provides an IEEE 802.3 compliant MDC/MDIO serial interface in master mode to get access to the registers in external PHYs.

The MDC frequency is configurable by modifying the value of **MDC/MDIO Clock Speed Register** (0x21153). Frame transmitted on the MDC/MDIO interface has the structure shown below. The order of the bit transmission shall be from left to right:

	Management Frame Fields						
	PRE(32bit)	ST	OP	PHY Addr	REG Addr	Data	IDLE
READ	1…….1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	$D_{15}D_{14}D_{13}$ …….$D_2D_1D_0$	Z
WRITE	1…….1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	$D_{15}D_{14}D_{13}$ …….$D_2D_1D_0$	Z

6. 18. Mirror Function

The **TF-480** provide six 16Kbyte program mirror memory blocks which share the TF-480's on chip 96K data memory. After copying program code from external flash to each of the internal mirror block and turn on the mirror function, the TF-480's internal CPU will fetch code in two cycles per instruction from the mirror block instead of fetching code from the external flash if the program counter is in the 16K range of any specific base address of each mirror.

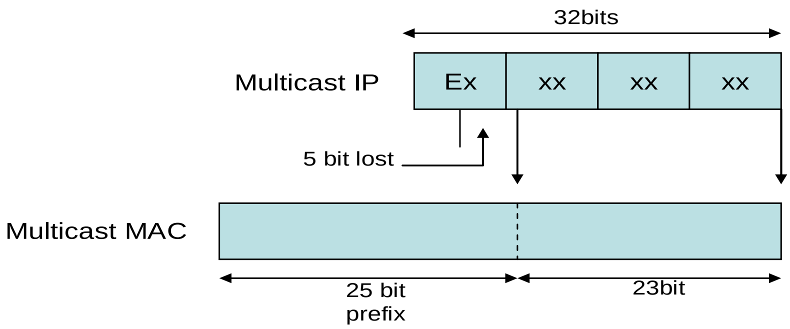


6. 19. WAN Rate Control

The **TF-480** provides rate control scheme on WAN port. Rate control scheme limits WAN port egress and ingress traffic to assigned data rates correspondingly. Egress data that exceeds the limit rate will be kept in the data buffer and wait for the data rate dropping below the assigned rate. Ingress data that exceeds the assigned data rate will be dropped. Data rates can be assigned separately for high priority traffic and low priority traffic if QoS is enabled.

6. 20. IP Multicast forwarding

The **TF-480** provides 32 IP multicast groups. Each group allows up to 32 multicast IP addresses which will be mapped to the same multicast MAC addresses. Bits[22:0] of the multicast IP address will define the multicast group, and the 32 variations of bits[27:23] will map to a 32 bit map of each group.



- Multicast IP = 32'hE000_0000~32'hEFFF_FFFF
- Multicast MAC = 48'h0100_5E00_0000~48'h0100_5E7F_FFFF
- IP[22:0] mapped to MAC[22:0], IP[31:28] is fixed number 4'hE, IP[27:23] is not mapped nor fixed
- MAC[47:23] is a fixed prefix with value 25'b0000_0001_0000_0000_0101_1110_0
- All the variations of IP[27:23] with the same value of IP[22:0] will mapped to the same multicast MAC address

We can also set all the 32 Multicast IP addresses of the same group (same IP[22:0]).

The IP multicast table is equipped with aging function for each group. A group should be set as static otherwise it will be aged out and removed by aging function. The aging function is default off.

If we want to see how the IP multicast is like, we can read an entry to see if it is valid and if it is static by giving a read entry command.

6. 21. I2C Slave

The TF-480 provides I2C as slave device. To enable this function, the TF-480 internal CPU must first configure the on chip I2C slave setup timer to a required value and the specific device address to the I2C Device Address register, then enable the I2C slave function. After the configuration is done, the external I2C master device can start to access the TF-480 internal I2C slave device.

I2C Data read format:

Start	ID[6:0]	write	Addr[23:16]	Addr[15:8]	Addr[7:0]	Stop

Start	ID[6:0]	read	Data_0[7:0]	Data_1[7:0]	…..	Data_n[7:0]	Stop

I2C Data write format

Start	ID[6:0]	write	Addr[23:16]	Addr[15:8]	Addr[7:0]	Data_0[7:0]	…	Data_n[7:0]	Stop

6. 22. Reverse MII

The LAN interface of **TF-480** can be configured as a reverse MII interface to directly connect to a switch by writing **RvMII enable** of **CPU Control Register 0.**

7. Electric Characteristics

7.1. Absolute Maximum Ratings (GND=0V)

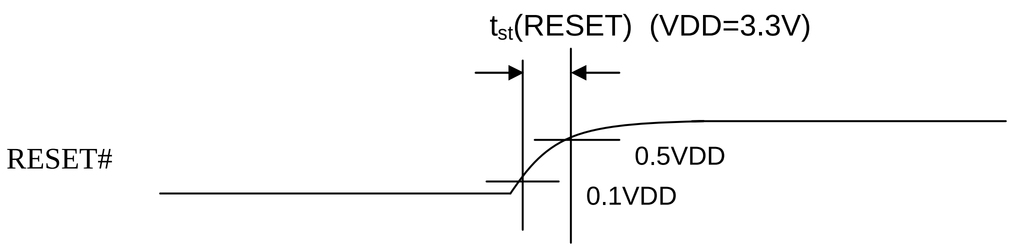
Item	Symbol	Conditions	Rating	Unit
Ambient Temperature	T_{AB}		0 °C to 70 °C	℃
Storage Temperature	T_{STG}		-60 °C to 150 °C	℃
Input Voltage	V_I		-0.3 to Vdd+0.5	V

7.2. DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
3.3V Power Supply	P-VDD		3.0	-	3.6	V
1.8V Power Supply	C-VDD		1.62	-	1.98	V
Input Low Voltage	V_{IL}		-	-	0.4	V
Input High Voltage	V_{IH}		2.4	-	-	V
Output Low Voltage	V_{OL}		-	-	0.4	V
Output High Voltage	V_{OL}		2.4	-	-	V
Input Leakage Current	I_{LI}	Input voltage = 0.4V	-10	-	10	uA
Input Pin Capacitance	C_I	f=1MHz, V_{DD}=0V	-	-	10	pF
Output Pin Capacitance	C_O	f=1MHz, V_{DD}=0V	-	-	10	pF
Input/Output Pin Capacitance	C_{IO}	f=1MHz, V_{DD}=0V	-	-	10	pF
3.3V Active Current	I_{DD}	f=50MHz	-	-	40	mA
1.8V Active Current	I_{DD}	f=50MHz	-	-	100	mA

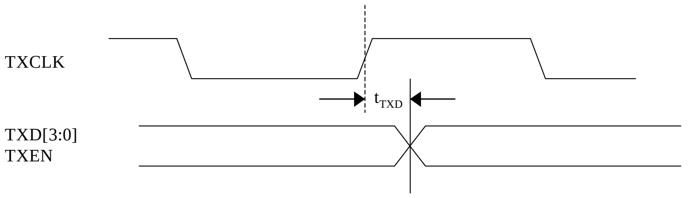
7.3. AC Characteristics Timing Chart

- **Reset Timing**

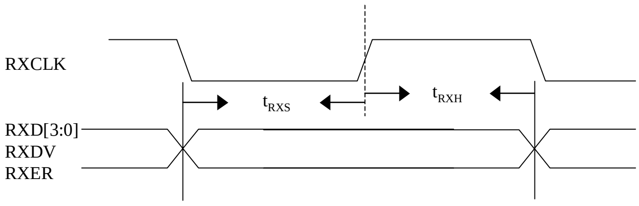


Item	Symbol	Min.	Max.	Unit
RESET time	t_{st}(RESET)	1		us

- **MII Interface**

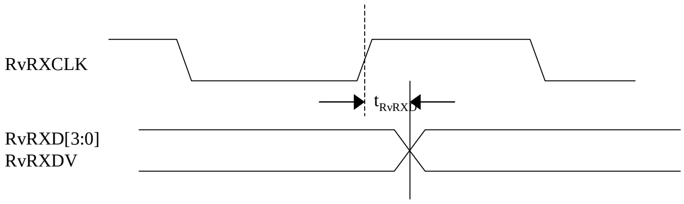


Item	Synbol	Min.	Max.	Unit
MII output data delay time	t_{TXD}		10	ns

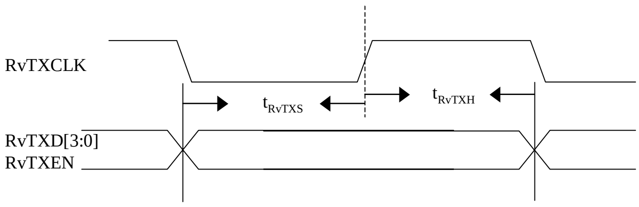


Item	Synbol	Min.	Max.	Unit
MII Input data setup time	t_{RXS}	5		ns
MII Input data hold time	t_{RXH}	2		ns

RvMII Interface

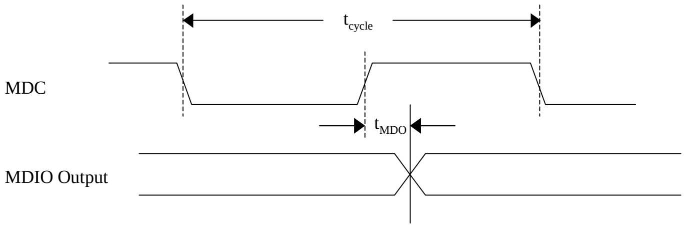


Item	Synbol	Min.	Max.	Unit
RvMII Output data (RX*) delay time	t_{RvRXD}	19	22	ns



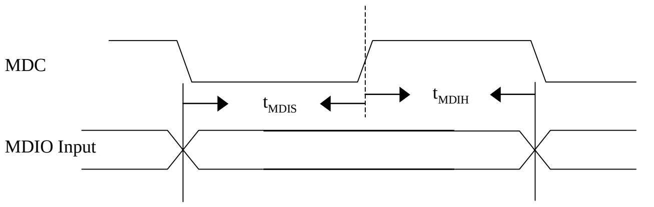
Item	Synbol	Min.	Max.	Unit
RvMII Input data (TX*) setup time	t_{RvTXS}	10		ns
RvMII Input data (TX*) hold time	t_{RvTXH}	0		ns

- **MDC/MDIO Interface**



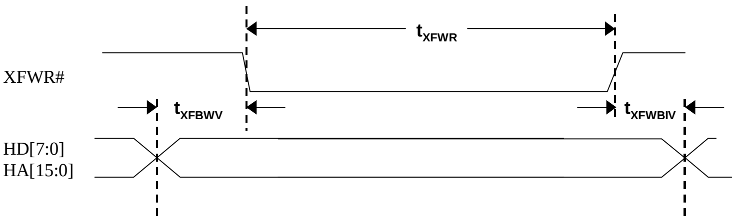
Item	Synbol	Min.	Max.	Unit
MDC/MDIO output data delay time	t_{MDO}	(t_{cycle} /2)	(t_{cycle} /2)+5	ns

Note: $\mathbf{t_{cycle}}$ is the cycle time of the MDC clock, which is configurable



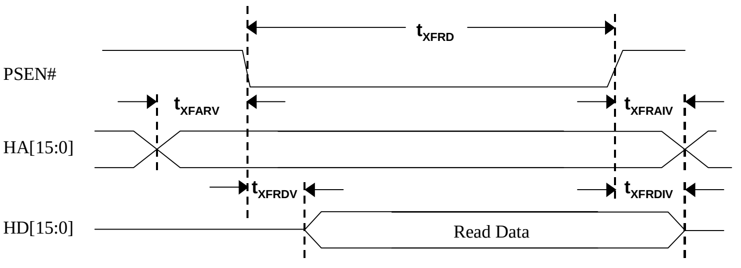
Item	Synbol	Min.	Max.	Unit
MDIO Input data setup time	t_{MDIS}	2		ns
MDIO Input data hold time	t_{MDIH}	0		ns

- **External Flash**



Item	Symbol	Min.	Max.	Unit
External Flash Write Assert Width	t_{XFWR}	T+nT	-	ns
Data/Address Bus valid to Write Assert	t_{XFBWV}	4	8	ns
Write de-assert to Data/Address Bus de-assert	t_{XFWBIV}	11	13	ns

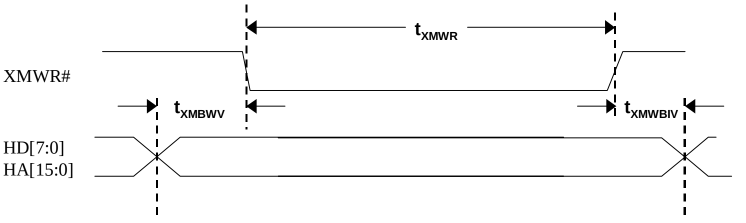
Note: **T** is the system clock cycle time.
n is the number of wait states.



Item	Symbol	Min.	Max.	Unit
External Flash Read Assert Width	t_{XFRD}	T+nT	-	ns
Address Bus valid to Read Assert	t_{XFARV}	16	20	ns
Read de-assert to Address Bus de-assert	t_{XFRAIV}	16	20	ns
Read assert to Data Bus assert	t_{XFRDV}	0	2+nT	ns
Read de-assert to Data Bus de-assert	t_{XFRDIV}	0	-	ns

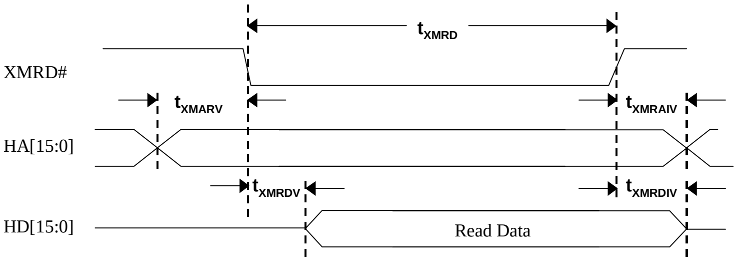
Note:
1. **T** is the system clock cycle time.
2. n is the number of wait states.
3. The value of n depends on the value of t_{XFRDV}, for example, the max t_{XFRDV} is 30, then we should choose wait state 2.

External RAM Interface



Item	Synbol	Min.	Max.	Unit
External Flash Write Assert Width	t_{XMWR}	T+nT	-	ns
Data/Address Bus valid to Write Assert	t_{XMBWV}	4	8	ns
Write de-assert to Data/Address Bus de-assert	t_{XMWBIV}	11	13	ns

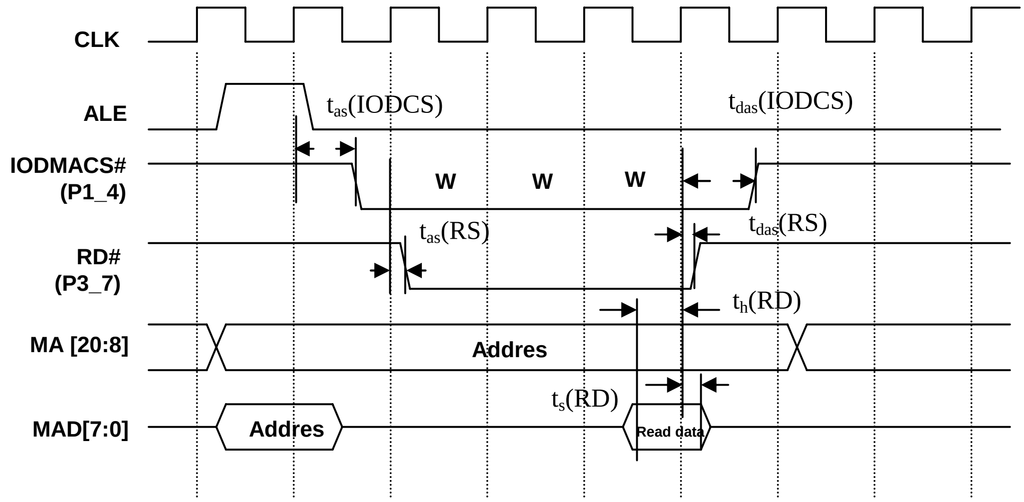
Note: **T** is the system clock cycle time.
n is the number of wait states.



Item	Synbol	Min.	Max.	Unit
External RAM Read Assert Width	t_{XMRD}	T+nT	-	ns
Address Bus valid to XRAM Read Assert	t_{XMARV}	16	26	ns
XRAM Read de-assert to Address Bus de-assert	t_{XMRAIV}	12	18	ns
XRAM Read assert to Data Bus assert	t_{XMRDV}	0	3+nT	ns
XRAM Read de-assert to Data Bus de-assert	t_{XMRDIV}	0	-	ns

Note:
1. **T** is the system clock cycle time.
2. n is the number of wait states.
3. The value of n depends on the value of t_{XFRDV}, for example, the max t_{XFRDV} is 30, then we should choose wait state 2.

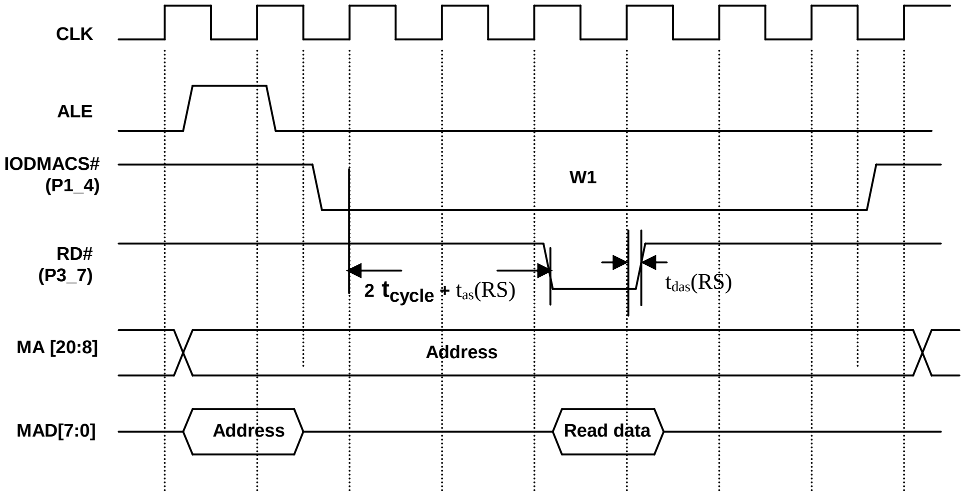
- **IO DMA Read Using Wait State Control (3 wait states)**



Item	Symbol	Min.	Max.	Note
IODMA Chip Select assert time	**t_{as}(IODCS)**	12	19	
IODMA Chip Select de-assert time	**t_{das}(IODCS)**	5	12	
IODMA Read Strobe assert time	**t_{as}(RS)**	5	12	
IODMA Read Strobe de-assert time	**t_{das}(RS)**	5	12	
Read Data Input data setup time	**t_s(RD)**	5	-	
Read Data Input data hold time	**t_h(RD)**	2	-	

- **IO DMA Read Using Wait State Control (3 wait states)**

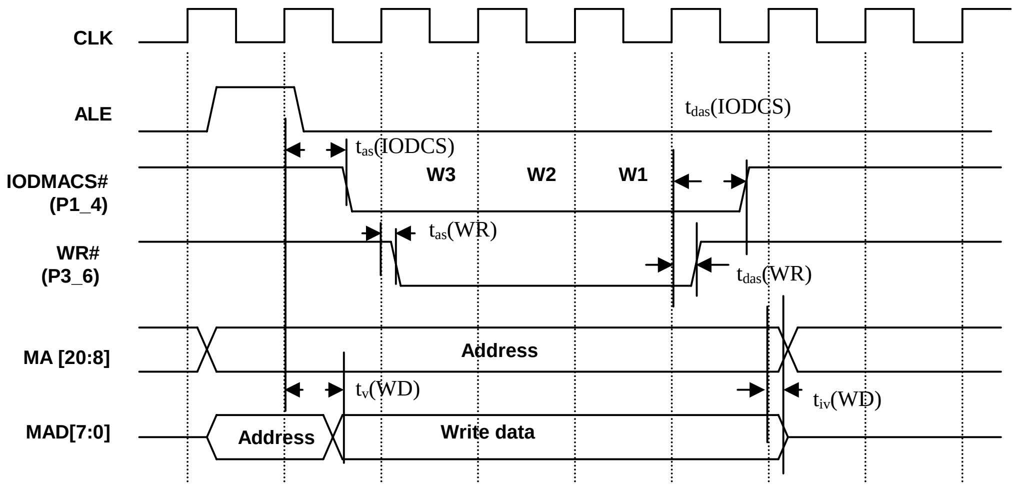
In the timing diagram, the access wait state is 1. And the IODMACS# falling to RD# falling, RD# rising to IODMACS# rising delay are 2 clocks.



Item	Symbol	Min.	Max.	Note
IODMA Read Strobe assert time	t_{as}(RS)	5	12	
IODMA Read Strobe de-assert time	t_{das}(RS)	5	12	

Note: t_{cycle} is the cycle time of the system clock

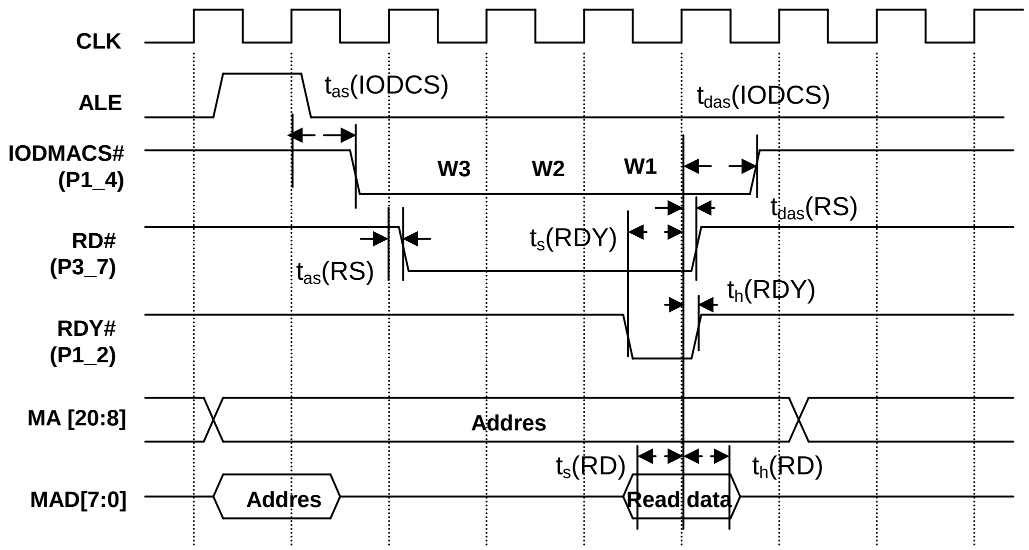
- **IO DMA Write Using Wait State Control (3 wait states)**



Item	Symbol	Min.	Max.	Note
IODMA Chip Select assert time	t_{as}(IODCS)	12	19	
IODMA Chip Select de-assert time	t_{das}(IODCS)	12	19	
IODMA Write Strobe assert time	t_{as}(WR)	5	12	
IODMA Write Strobe de-assert time	t_{das}(WR)	5	12	
Write Data valid time	t_v(WD)	11.5	19	
Write Data invalid time	t_{iv}(WD)	10	-	

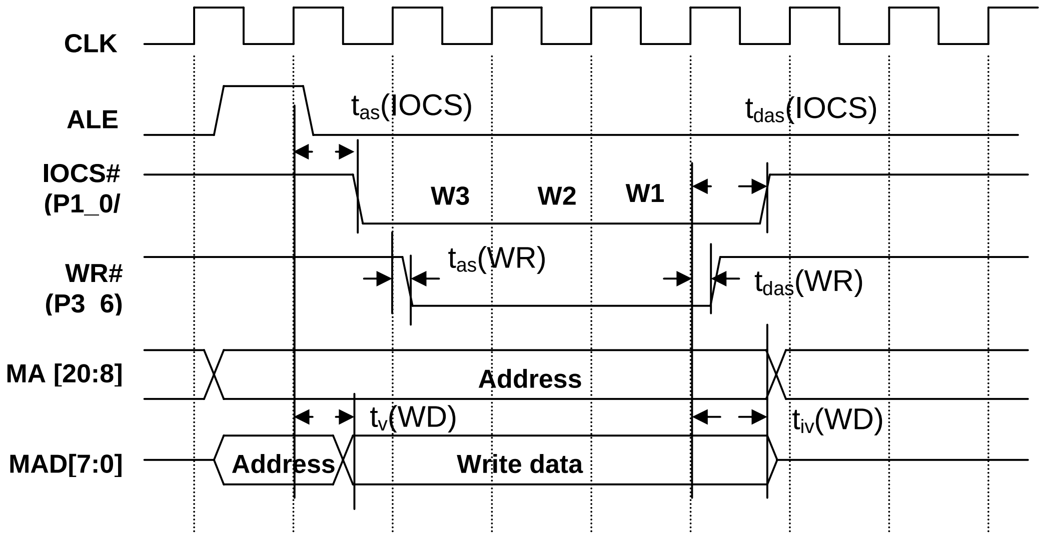
IO DMA Read Using External RDY Control

In this timing diagram, the access wait state is 3. The IOCS# falling to RD# falling, RD# rising to IOCS# rising delay are no effect for this access.



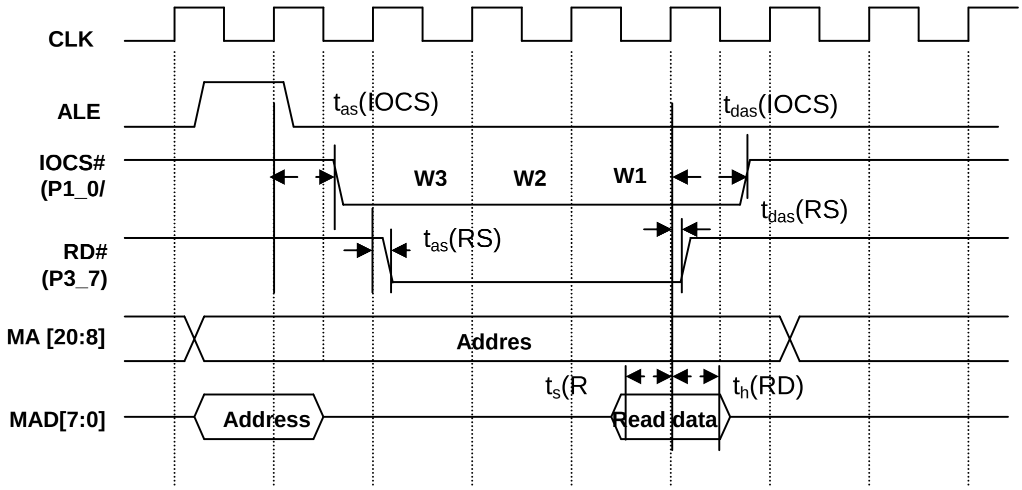
Item	Symbol	Min.	Max.	Note
IODMA Chip Select assert time	t_{as}(IODCS)	12	19	
IODMA Chip Select de-assert time	t_{das}(IODCS)	5	12	
IODMA Read Strobe assert time	t_{as}(RS)	5	12	
IODMA Read Strobe de-assert time	t_{das}(RS)	5	12	
RDY input setup time	t_s(RDY)	5	-	
RDY input hold time	t_h(RDY)	2	-	
Read Data Input data setup time	t_s(RD)	5	-	
Read Data Input data hold time	t_h(RD)	2	-	

- **Extended IO Write Using Wait State Control (3 wait states)**



Item	Symbol	Min.	Max.	Note
IODMA Chip Select assert time	t_{as}(IOCS)	12	19	
IODMA Chip Select de-assert time	t_{das}(IOCS)	12	19	
IODMA Write Strobe assert time	t_{as}(WR)	5	12	
IODMA Write Strobe de-assert time	t_{das}(WR)	5	12	
Write Data valid delay time	t_{v}(WD)	11.5	19	
Write Data invalid delay time	t_{iv}(WD)	10	-	

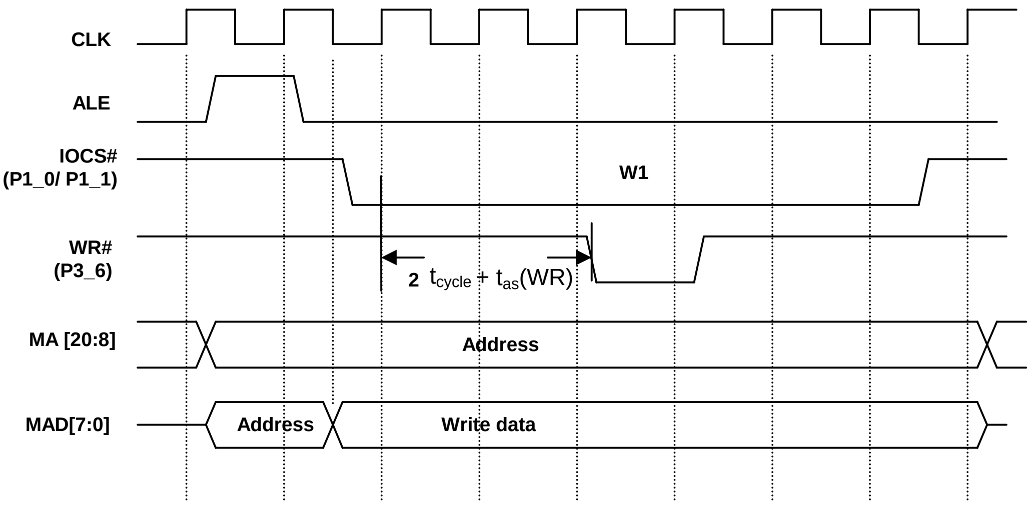
- **Extended IO Read Using Wait State Control**



Item	Symbol	Min.	Max.	Note
IODMA Chip Select assert time	t_{as}(IOCS)	12	19	
IODMA Chip Select de-assert time	t_{das}(IOCS)	5	12	
IODMA Read Strobe assert time	t_{as}(RS)	5	12	
IODMA Read Strobe de-assert time	t_{das}(RS)	5	12	
RDY input setup time	t_s(RDY)	5	-	
RDY input hold time	t_h(RDY)	2	-	
Read Data Input data setup time	t_s(RD)	5	-	
Read Data Input data hold time	t_h(RD)	2	-	

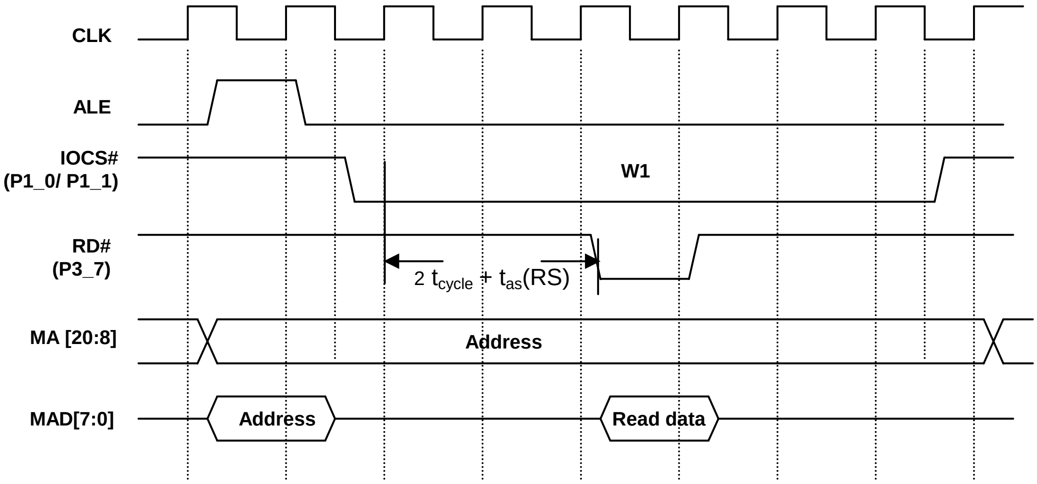
- **Extended IO Write Using Wait State Control with Delay Control**

In this timing diagram, the wait state is 1, and IOCS# falling to WR# falling and WR# rising to IOCS# rising delay is 2 system clocks.

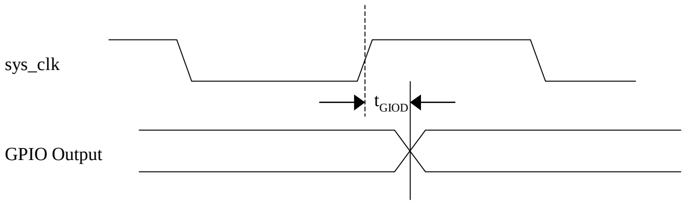


- **Extended IO Read Using Wait State Control with Delay Control**

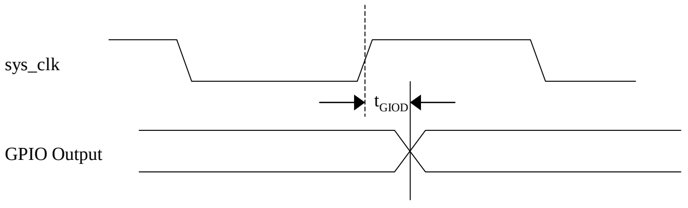
In this timing diagram, the wait state is 1, and IOCS# falling to WR# falling and WR# rising to IOCS# rising delay is 2 system clocks.



- **GPIO Interface**



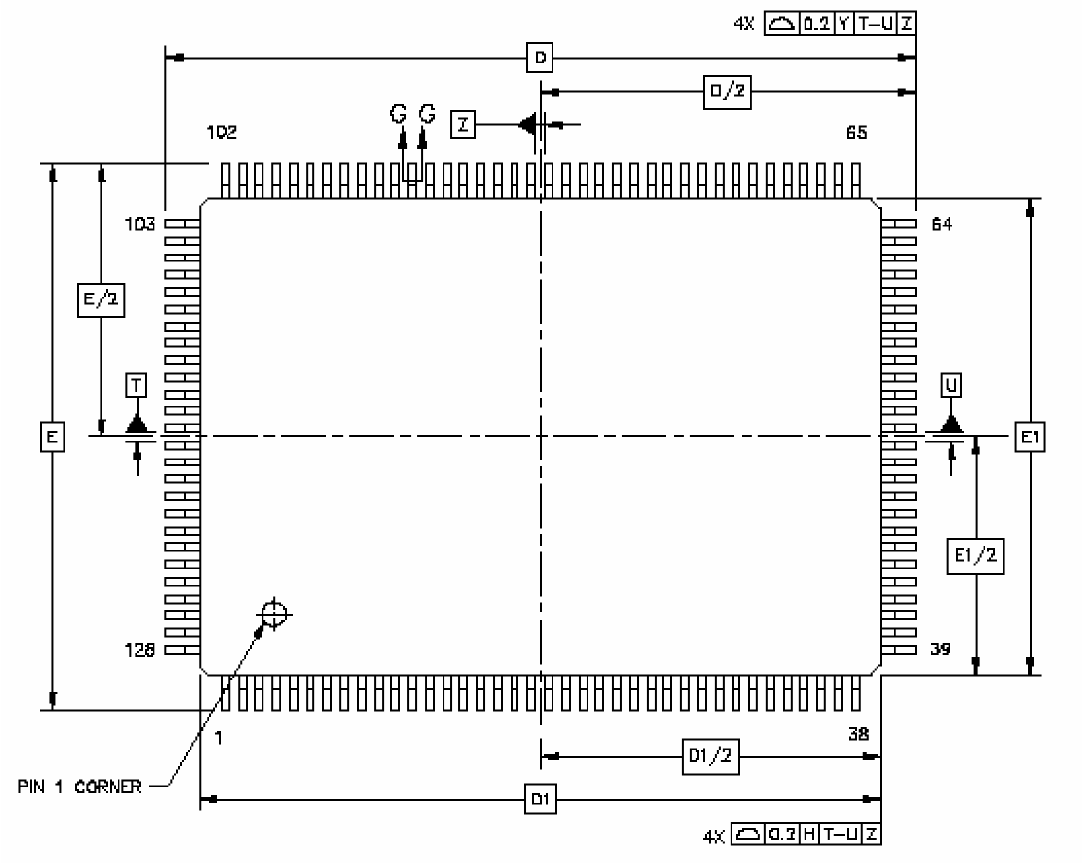
Item	Synbol	Min.	Max.	Unit
GPIO Output data delay time	t_{GIOD}		15	ns

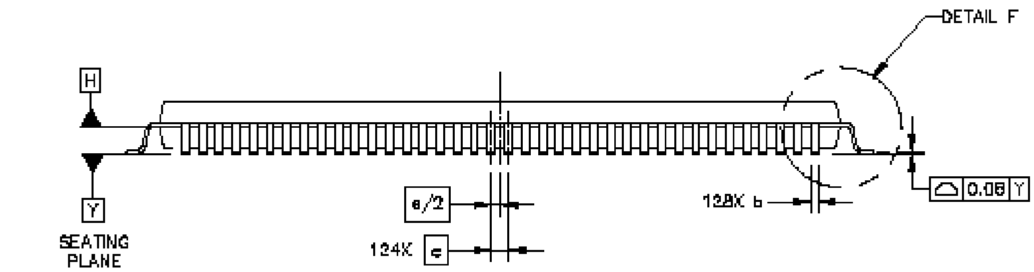


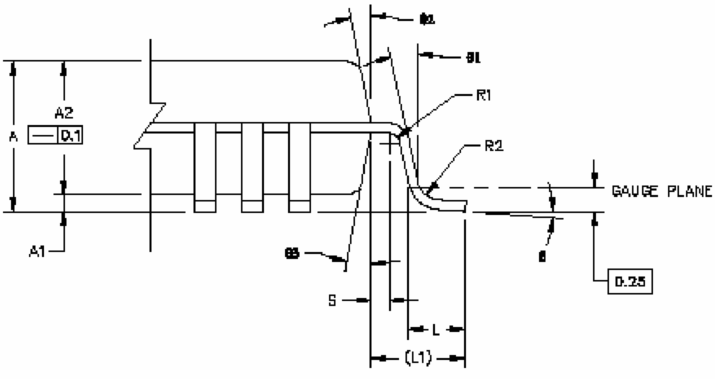
Item	Synbol	Min.	Max.	Unit
GPIO Output data delay time	t_{GIOD}		15	ns

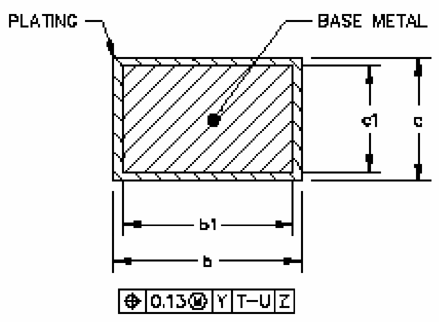
8. Mechanical Dimensions

128-Pin PQFP -- Plastic QFP 128pin Body size 20 x 14 x 2.8 mm






A
A2
0.1
A1
R1
R2
GAUGE PLANE
0.25
S
L
(L1)


PLATING
BASE METAL
c1
c
b1
b
0.13 M Y T-U Z

SYMBOL	DIMENSION (MM)			DIMENSION (ML)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			3.40			134
A1	0,25			10		
A2	2.55	2.80	3.05	100	110	120
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.13		0.23	5		9
c1	0.13		0.17	5		7
D	22.95	23.20	23.45	904	913	923
D1	19.90	20.00	21.10	784	787	791
E	16.95	17.20	17.45	667	677	687
E1	13.90	14.00	14.10	547	551	555
e	0.50 BSC			20 BSC		
L	0.73	0.88	1.03	29	35	41
L1	1.6 REF			63 REF		
R1	0.13			5		
R2	0.13		0.30	5		12
Y			0.075			3
θ	0^{o}		7^{o}	0^{o}		7^{o}
θ1	0^{o}			0^{o}		
θ2	5^{o}		16^{o}	5^{o}		16^{o}
θ3	5^{o}		16^{o}	5^{o}		16^{o}